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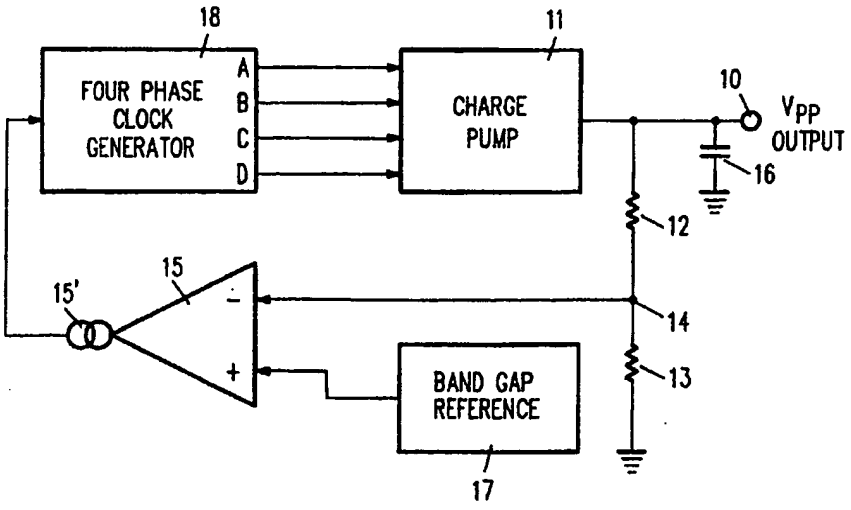

(57) Abstract

A high-voltage generator circuit produces a high voltage that is employed in the operation of an electrically-erasable, programmable read only memory. The circuit is described for MOS implementation as an on chip construction. A charge pump composed of a plurality of stages is driven by a plural-phase-clock-signal operated from a four-phase clock-signal generator which has a frequency determined by an input current. A comparator having an output current that is related to a differential input displays a truncated response; the output current is zero for zero differential input and a maximum output current when the noninverting input potential substantially exceeds the inverting input potential. The noninverting input is coupled to a reference potential and the inverting input is coupled to receive a controlled fraction of the high voltage produced by the charge pump. At start-up, the high voltage is zero and the comparator applies a maximum current to the clock generator which thereby operates at maximum frequency and minimizes startup time. After start-up, the clock frequency will be proportional to the current drawn from the high-voltage generator circuit.

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CONSTANT HIGH VOLTAGE GENERATOR

Background of the Invention

The invention broadly relates to electrically erasable programmable read only memory (EEPROM) devices. It specifically is directed to the V_{pp} high voltage generator employed for such devices. V_{pp} is typically about 15 volts produced by a charge pump in an on-chip integrated circuit configuration. A charge pump is ordinarily employed to boost the typically 3- or 5-volt operating supply to the desired value. Desirably, the charge pump and other chip circuits should be operative down to about a 2 volt supply level and be capable of producing the 15 volt V_{pp}.

This invention makes use of a copending patent application, serial no. 08/070,614, filed 02 June, 1993, titled SELF-TIMING FOUR-PHASE CLOCK GENERATOR. This application is directed to a clock generator having four phases that are employed to drive a charge-pump high-voltage generator. The clock frequency is directly proportional to an input current. The teaching in this application is incorporared herein by reference.

Summary of the Invention

It is an object of the invention to produce a controlled high-voltage level by means of a charge pump driven from a current-sensitive clock generator.

It is a further object of the invention to produce a frequency-controlled, high-voltage generator by means of a charge pump driven from a variable-frequency, current-sensitive, clock-signal generator which responds to a current-pro-

duce a frequency-controlled, high-voltage generator by means of a charge pump driven from a variable-frequency, current-sensitive, clock-signal generator which responds to a current-producing comparator.

These and other objects are achieved in the following manner. A plural-stage charge pump is driven from a plural-phase clock-signal generator which produces a clock frequency that is proportional to an input current. The high voltage is applied to a voltage divider, the output of which is connected to the inverting input of a comparator having an output current proportional to the differential input. The non-inverting comparator input is connected to a band-gap reference potential source which provides a stable, temperature- and supply-voltage independent reference voltage. At startup, when V_{PP} is zero, the comparator output current will saturate at its highest value because of the large difference in input voltages. The clock oscillator will be driven to its highest frequency as a result. Since a charge pump will develop an elevated output after a number of clock cycles, its output will quickly rise. When V_{PP} has risen to its desired value and the voltage-divider output has risen to equal the band-gap reference potential, the comparator output current will go to zero and the clock will stop. As long as V_{PP} is at its desired value, the comparator output will remain at zero. However, when current is drawn from V_{PP}, the V_{PP} level will begin to fall and the comparator will produce an output current so that the clock generator will produce a clock signal. The clock frequency will be adjusted by the feedback circuit so that the charge pump will

replenish the drop in V_{PP} due to current drain. Thus, the charge-pump frequency will be controlled so that the desired V_{PP} level is maintained, independent of the magnitude of current drain.

Brief Description of the Drawing

Figure 1 is a block diagram of the overall V_{PP} voltage-regulator circuit.

Figure 2 is a graph showing the truncated response of the voltage comparator.

Figure 3 is a graph showing the waveforms for a four-phase clock signal.

Figure 4 is a schematic diagram of a charge-pump element.

Figure 5 is a block diagram of a charge pump suitable for use in the figure 1 block diagram.

Description of the Invention

With reference to figure 1, which is a block diagram of a V_{PP} voltage generator, the output voltage appears at terminal 10. Capacitor 16 is the V_{PP} output voltage supply filter capacitor. The V_{PP} output is developed by a charge pump 11 which will be described in more detail subsequently. A voltage divider, composed of resistors 12 and 13, produces a controlled fraction of V_{PP} at node 14. In a typical system, this fraction is about 1/12.5. This fraction is applied to the inverting input of comparator 15 which provides a controlled-current output as shown by current source 15'. A band gap-reference 17 is connected to the noninverting input of comparator 15. Comparator 15 applies a current to a four-phase clock generator

capacitance. Transistor 30 is one of the bucket-brigade capacitances that contributes charge to be V_{PP} output current. Transistor 29 serves only to aid the charging of the gate of transistor 27.

The second pump element, which receives clocks A and D, is composed of N channel transistors 31 and 32. N channel depletion transistors 33 and 34 have their source and drain electrodes shorted together so that they too function as capacitors. Transistor 34 is made larger than transistor 33 by a factor in excess of about 40 so that it provides a proportionately larger capacitance.

As can be seen from figure 3, clocks B and D are alternately high so that transistors 27 and 31 are alternately turned on. Transistor 27 will charge capacitor 30 during the time interval when clock C is low. It will be noted that when clock C is initially driven low, node 22 is pulled down thereby turning transistor 28 off. Thus, capacitor 30 will charge. Then, when clock C goes high, node 22 will rise and turn transistor 28 on, so that the gate of transistor 27 is connected to its drain. In this state, transistor 27 will be unilaterally conductive so that capacitor 30 cannot discharge through transistor 27. This action traps the charge on capacitor 30. After a sufficient number of clock cycles, node 22 will rise and approach a level of about the potential at terminal 20 plus a substantial portion of the peak voltage of clock C.

After capacitor 30 has been incrementally charged, clock D will go high and capacitor 33 will couple

the pulse to transistor 31 so as to turn it on. This occurs after clock A goes low so as to pull terminal 21 low, thereby turning transistor 32 off. During the clock D high, capacitor 34 will charge through transistor 31 from node 22. Then, when clock A goes high, the pulse at terminal 21 will turn transistor 32 on so that the gate of transistor 31 is returned to its drain thereby rendering transistor 31 unidirectionally conductive and the charge on capacitor 34 will be blocked. After a sufficient number of clock cycles, capacitor 34 will charge to a level approaching the clock A peak value above the level of node 22. Thus, a nearly clock peak voltage will be added to the nearly peak voltage at node 22. Thus, an increment of nearly two clock peak voltages will be developed at terminal 21.

Clearly, a number of figure 4 stages can be cascaded so as to develop any desired output voltage. As shown in the block diagram of figure 5, seven such stages comprise block 11 of figure 1. These stages are shown being operated from the four clock phases from generator 18. Each of pump stages 36 through 42 comprise the circuit of figure 3. With this number of stages, the circuit of figure 3 can easily operate down to a two volt V_{DD} level. A two volt input at terminal 20 needs to be multiplied only 7.5 times to achieve a 15 volt V_{PP}. The seven stages shown can provide this output after a relatively few number of clock cycles. N channel transistor 43, which has its gate connected to its drain, acts as a one way coupling device that will pass the positive voltage out of pump element 42 to terminal 10.

The invention has been described and a preferred

embodiment detailed. When a person skilled in the art reads the foregoing description, alternatives and equivalents, within the spirit and intent of the invention, will be apparent. Accordingly, it is intended that the scope of the invention be limited only by the claims that follow.

I claim:

1. A high-voltage generator circuit for use with electrically erasable programmable read only memory systems, said circuit comprising:

a plural-phase-clock-signal generator for generating clock phases in response to a current input;

a charge pump responsive to said plural phase clock signal to produce said high voltage; and

a comparator having an output current coupled to said clock-signal generator, a noninverting input coupled to a source of reference potential and an inverting input coupled to receive a controlled fraction of said high voltage whereby said circuit produces a stable operating condition wherein said fraction of said high voltage substantially equals said reference potential.

2. The high voltage generator circuit of claim 1 wherein said comparator current controls the frequency of said clock signal generator.

3. The high voltage generator circuit of claim 2 wherein said comparator has a truncated response of zero for the condition of equal input voltages and a substantial-value maximum current when said noninverting input substantially exceeds said inverting input.

4. The high-voltage generator circuit of claim 3 wherein said clock generator frequency is zero when said comparator noninverting and inverting inputs are at the same potential.

5. The high voltage generator circuit of claim 4 wherein the extraction of current from said high voltage generator circuit acts to reduce said high voltage whereby unbalance of said comparator provides a current to said clock generator which in turn operates said charge pump thereby ensuring a charge pump operating frequency that is proportional to said extraction of current.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 94/06022

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 G11C16/06 H02M3/07

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 G11C H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	WO,A,93 14555 (SIERRA SEMICONDUCTOR BV) 22 July 1993	1,2
P,A	see page 4, line 27 - page 5, line 10; claim 1; figure 1	3-5
Y	GB,A,2 035 629 (RCA CORPORATION) 18 June 1980	1,2
A	see the whole document	3-5
Y	EP,A,0 297 545 (HITACHI LTD) 4 January 1989	1,2
A	see column 4, line 35 - column 8, line 55; figures 1-5	5
A	US,A,4 631 421 (INOUE ET AL) 23 December 1986 see column 1, line 61 - column 2, line 26; figures	1-4

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
12 September 1994	05.10.94

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Cummings, A

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 94/06022

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 350 462 (SGS-THOMSON MICROELECTRONICS SRL) 10 January 1990 see column 3, line 21 - column 4, line 65; figure 2 ---	1,2,4
A	IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE., vol.35, February 1992, NEW YORK US pages 152 - 153 KURIYAMA ET AL 'A 5V-only 0.6um Flash EEPROM with row decoder scheme in triple-well structure' see figure 3 -----	1

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US 94/06022

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